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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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SPRINKLE IP LAW GROUP
1301 W. 25TH STREET
SUITE 408
AUSTIN, TX 78705

EXAMINER	
CHANG, RICHARD	
ART UNIT	**PAPER NUMBER**
2663	

DATE MAILED: 07/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

SM

Office Action Summary	Application No.	Applicant(s)	
	09/886,518	SOMASHEKHAR, HOSAGRAHAR	
	Examiner	Art Unit	
	Richard Chang	2663	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,7-12,20,21 and 25* is/are rejected.

7)☒ Claim(s) *2-6,13-19,22-24 and 26-31* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Applicant's arguments and amendments with respect to claims 1-31 have been fully considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1 and 7-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over US patent 6,347,234 ("Schwartz et al.") in view of US patent No. 6,781,984 ("Adam et al.").

Regarding claim 1, Schwartz et al. teach a systems and methods for switching packets of digital data in a switching node used in a digital data network (a system for transporting data from a plurality ingress to a plurality of egress line) (See Fig. 2, Col. 5, lines 5-8) comprising of

an inter-port packet switch (22, data switching matrix), in the form of a crosspoint switch, having a plurality of input ports coupled to of input port modules (20(n)) and a plurality of output coupled to of output port modules (21(n)) wherein for each of the ingress ports, the data switching matrix is configured to transport data from each the ingress port to one of the plurality of egress ports (See Fig. 2, Col. 5, lines 48-50),

a number of input port modules (20(1) through 20(N), a plurality of ingress edge units), each of which is coupled to one of the plurality of ingress ports of the an inter-port packet switch (22, data switching matrix), wherein each of the plurality of ingress edge units is configured to receive a data from a corresponding input ports (25(n)(1) through 25(n)(M), one or more of a plurality of ingress lines) (See Fig. 2, Col. 5, lines 12-17),

a number of output port modules (21(1) through 21(N), a plurality of egress edge units), each of which is coupled to one of the plurality of egress ports of the an inter-port packet switch (22, data switching matrix), wherein each of the plurality of egress edge units is configured to transmit data received from the data switching matrix to a plurality of output (egress) ports (26(n)(1) through 26(n)(M), one or more of a plurality of egress lines) (See Fig. 2, Col. 5, lines 24-29),

wherein, for each packet received, the input port module (20(n), each of the plurality of ingress edge units) is configured to identifies from the destination address contained in the each received packet's header (examine data received ... and to identify portions of the data ...egress edge units),

wherein the packet (portions of the data) corresponding to each of the output port module (21(n), egress edge units) is stored in a corresponding buffer and wherein data in each buffer is transmitted to the corresponding egress edge unit (21(n)) via the inter-port packet switch (22, data switching matrix) corresponding to real time meta-data packet control signals (in a predetermined time slots) (See Fig. 2, Col. 5, lines 21-31).

Schwartz et al. teaches substantially all the claimed invention but did not disclose expressly the particular application involving limitations of

"input packet buffers synchronization and output packet buffer synchronization being correlated via time distribution block".

Adam et al. teaches that input packet buffers (206) synchronization (208) and output packet buffer (214) synchronization (216) being correlated via time distribution block (See Fig. 2, Col. 3, lines 20-34).

A person of ordinary skill in the art would have been motivated to employ Adam et al. in Schwartz et al. in order to obtain a systems and methods for switching packets of digital data in a switching node used in a digital data network and to take advantage of input packet buffers synchronization and output packet buffer synchronization being correlated via time distribution block in claim 1.

The suggestion/motivation to do so would have been to correlate input packet buffers synchronization and output packet buffer synchronization being via time distribution block, as suggested by Adam et al. in Col. 3, lines 20-34. At the time the invention was made, therefore, it would have been obvious to one of ordinary skill in the art to which the invention pertains to combine Adam et al. with the Schwartz et al. to obtain the inventions specified in claim 1.

Regarding claim 11, this claim has limitations that is similar to those of claim 1 and Schwartz et al. further teach that there is a plurality of e buffers of the packets received from the network interface (30) in the packet memory (31) for all input (ingress) ports 25(n) in the input port module 20(n), and the control circuit (33) may also receives

packet transfer requests directly via a packet segment generator (34) to controls retrieval and transfer of packets from the packet memory (31) to the inter-port packet switch (22) for transfer to the output port modules 21(n) (independent of the predetermined time slot) (See Fig. 2, Col. 10, lines 30-35), thus it is rejected with the same rationale applied against claim 1 above.

Regarding claims 7-8 and 12, these claims have limitations that is similar to those of claims 1 and 11 and Schwartz et al. further teach that the communication links 13(p) may utilize any convenient information transmission medium including optical fiber links for carrying optical signals (See Fig. 1, Col. 5, lines 18-21), thus it is rejected with the same rationale applied against claims 1 and 11 above.

Regarding claim 9-10, these claims have limitations that is similar to those of claims 1 and 11 and Schwartz et al. further teach that the input port module 20(n) has a plurality of input (ingress) ports (25(n)(1) through 25(n)(M)) which are connected to respective one of the communication links 13(p) for receiving packets (component with line function) (See Fig. 2, Col. 5, lines 15-20) and function modules to transfer the packet to the switching fabric (component with service function) (See Fig. 2, Col. 5, lines 32-35), thus it is rejected with the same rationale applied against claims 1 and 11 above.

4. Claims 20-21 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over US patent No. 5,126,999 ("Munter et al.") in view of US patent No. 6,781,984 ("Adam et al.").

Regarding claims 20 and 21, Munter et al. teach a method for high speed packet switching and to space-division switching by means of input-buffered NxN switching or cross-point matrices (a method for transporting data) (See Fig. 1 and Fig. 3, Col. 5, lines 25-27) comprising of

demultiplexing (parsing) each incoming data stream (received data stream) header in header decoder (41) into the appropriate packet (a plurality of data cells) (See Fig. 4, Col. 5, lines 58-60),

decoding (identifying) the packet (plurality of data cells) header in header decoder (41) for packet's switch output port destination (See Fig. 4, Col. 5, lines 63-66),

storing (segregating) the packets (plurality of data cells) into the plural FIFOs (F1 to F16, distinct sets of data cells)

based on the packet's switch output port destination (wherein the data set of a plurality of data cells has a common destination)) (See Fig. 4, Col. 5, lines 58-63), and

operating dynamically on a real-time basis (sequentially transmitting) by means of an N crosspoint selector (33) to yield a new selection of N crosspoints in the switch (30) for connection of the input packets and buffers (distinct sets of a plurality of data cells) to the corresponding destinations (See Fig. 3, Col. 5, lines 30-40).

Munter et al. teaches substantially all the claimed invention but did not disclose expressly the particular application involving limitations of

"input packet buffers synchronization and output packet buffer synchronization being correlated via time distribution block".

Adam et al. teaches that input packet buffers (206) synchronization (208) and output packet buffer (214) synchronization (216) being correlated via time distribution block (See Fig. 2, Col. 3, lines 20-34).

A person of ordinary skill in the art would have been motivated to employ Adam et al. in Munter et al. in order to obtain a systems and methods for switching packets of digital data in a switching node used in a digital data network and to take advantage of input packet buffers synchronization and output packet buffer synchronization being correlated via time distribution block in claim 1.

The suggestion/motivation to do so would have been to correlate input packet buffers synchronization and output packet buffer synchronization being via time distribution block, as suggested by Adam et al. in Col. 3, lines 20-34. At the time the invention was made, therefore, it would have been obvious to one of ordinary skill in the art to which the invention pertains to combine Adam et al. with the Munter et al. to obtain the inventions specified in claim 1.

Regarding claim 25, this claim has limitations that is similar to those of claim 21 and Munter et al. further teach that storing (segregating) the packets (plurality of data cells) into plural FIFOs (F1 to F16, distinct sets of data cells) having the same packet's switch output port destination (wherein the data set of a plurality of data cells has a common destination) (See Fig. 4, Col. 5, lines 58-63), thus it is rejected with the same rationale applied against claim 21 above.

Allowable Subject Matter

5. Claims 2-6, 13-19,22-24 and 26-31 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims and if no art rejection can be applied.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Richard Chang whose telephone number is (571) 272-3129. The examiner can normally be reached on Monday - Friday from 8 AM to 5 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ricky Ngo can be reached on (571) 272-3139. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

rkc

Richard Chang
Patent Examiner
Art Unit 2663

RICKY NGO
PRIMARY EXAMINER

7/11/05